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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/456,230	12/07/99	WAKAYAMA M	36159/JWE/B6

EXAMINER	
TRAN, A	
ART UNIT	**PAPER NUMBER**
2816	

MMC2/1205
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DATE MAILED: 12/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/456,230	WAKAYAMA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghoshal (USP 5068628) in view of Hsu (USP 5805003).

As to claims 1 and 2, Ghoshal shows in figure 2 a phase lock loop comprising: a detector (76) for comparing a phase or frequency characteristic of an input signal (26) to a phase or frequency characteristic of a timing reference signal (74); a timing reference signal generator (46, 48,..., 56, 78), connected in feedback fashion to provide a timing reference signal to the detector. Thus, figure 2 shows all elements of the claim except for the timing reference signal generator is operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency. However, Hsu shows in figure 1 a frequency divider circuit (/M) for reducing the output frequency. Therefore, it would have been obvious to one having ordinary skill in the art to add a frequency divider circuit to the output of Ghoshal's figure 2 for the purpose of reducing the output frequency.

As to claim 3, Ghoshal's figure 2 shows block 76 further comprises a loop filter.

As to claim 4, Ghoshal's figure 2 shows the timing reference generator is constructed to output multi-phase signals (58, 60, ..., 68), each phase signal oscillating at the characteristic frequency.

As to claim 5, Ghoshal's figure 2 shows a phase select MUX (78), the phase select MUX selecting between and among the multiphase signals to define a respective one as an output clock signal.

As to claim 6, the reference of Ghashal and Hsu teach that the timing reference signal generator is operatively configured to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency.

As to claim 7, the reference of Ghoshal and Hsu teach that the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

Claim 12 is rejected as being inherent from the rejections above.

As to claim 13, the reference of Ghoshal and Hsu teach that the desired output clock signal has a frequency characteristic N times the frequency characteristic of the input signal (it is understand that N can be any value).

As to claim 14, Ghoshal's figure 2 shows a first frequency divider circuitry (72) disposed between the timing reference signal generator and the comparison circuit; and Hsu's figure 21 shows a second frequency divider circuitry (/M) disposed between the timing reference signal generator and an output (see the rejection of claim 1), wherein the first and second frequency divider circuitry having different frequency division characteristics.

As to claim 15, the reference of Ghoshal and Hsu teach that the first frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor

(NxM) (wherin N can be any value) to develop the frequency characteristic provided to the comparison circuit.

As to claim 16, Hsu's figure 1 shows the second frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor M to develop the desired output clock signal.

As to claim 17, Ghoshal's figure 2 shows the timing reference signal generator is implemented as a VCO, the VCO constructed as a sequential delay stage (46, 48, ..., 56).

As to claim 18, Ghoshal's figure 2 the VCO developing multi-phase output signals (58, 60, ..., 68), each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage.

As to claim 19, the reference of Ghoshal and Hsu teach the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

As to claim 20, Ghoshal's figure 2 shows a phase select MUX (78), the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal.

3. Claims 8-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghoshal (USP 5068628) in view of Hsu (USP 5805003) and Barrett et al. (USP 5243599).

As to claims 8 and 21, the reference of Ghoshal's figure 2 and Hsu's figure 1 show all elements of claim 8 except for the phase select MUX is a Gray code MUX. However, Barrett et al. shows in figure 3 a Gray code MUX with the advantage of providing faster control path than

other types of decode devices. Therfore, it would have been obvious to one having ordinary skill in the art to employ the teaching of Barrett et al. in to the Ghoshal's MUX for the purpose of having faster control path.

As to claims 9 and 22, Barrett et al.'s figure 3 shows the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

As to claim 10, it is seen as an obvious design choice for selecting frequency divider circuit to be constructed of current mode logic components dependent upon the environment of use to ensure optimum performance.

As to claim 11, it is seen as an obvious design choice for selecting phase control MUX to be constructed of current mode logic components dependent upon the environment of use to ensure optimum performance.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
November 30, 2000

Terry D. Cunningham
Primary Examiner